Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-49 (canceled)

50. (currently amended) A method for forming conducting structures separated by gaps on a substrate comprising:

providing a substrate and a wiring line layer above the substrate;

providing a conductive layer on the wiring line layer;

forming a cap layer [[above]] <u>on</u> the conductive layer, wherein said cap layer has ~~a uniform~~ <u>no more than minor variations in</u> thickness and <u>the cap layer has</u> a composition adapted to provide a graded index of refraction between said conductive layer and a photoresist layer during a photolithographic process, the photoresist layer being formed on top of the cap layer;

etching through a portion of the cap layer and portions of the conductive layer and wiring line layer to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon; and

depositing a dielectric material on surfaces exposed by the etching process including exposed surfaces of the cap layer to substantially fill the gaps between the wiring lines, said dielectric material including a layer formed by high density plasma chemical vapor deposition,

wherein the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of depositing the dielectric material.

51. (previously presented) The method of claim 50, wherein the cap layer is used as a hard mask during etching of the wiring line layer.

52. (previously presented) The method of claim 50, wherein the cap layer comprises an antireflective coating that operates by destructive interference, and said conductive layer comprises an antireflective coating that operates by absorption.

53. (previously presented) The method of claim 50, wherein portions of the cap layer are partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition.

54. (previously presented) The method of claim 50, wherein the cap layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

55. (previously presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has a rectangular shape in cross section.

56. (previously presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has a trapezoidal shape in cross section.

57. (previously presented) The method of claim 56, wherein the trapezoidal shape includes top and bottom surfaces parallel to one another and side surfaces that extend inwardly from the bottom surface to the top surface.

58. (previously presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has a triangular shape in cross section.

59. (previously presented) The method of claim 50, wherein the remaining portion of the cap layer on at least one wiring line has, in cross section, a rectangular shape having its upper corners etched away.

60. (previously presented) The method of claim 50, wherein the remaining portion of the cap layer is adapted during an etch operation to have a shape that reduces redeposition of the cap layer into the gaps during the high density plasma chemical vapor deposition process.

61. (currently amended) A method of forming conducting structures separated by gaps filled with dielectric material, comprising the steps of:

providing a substrate containing silicon, the substrate having a surface;

forming a surface layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten alloy, the surface layer disposed on the substrate surface;

forming a metal wiring layer on the surface layer, the metal wiring layer having an upper surface;

forming a protective layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten alloy, the protective layer disposed on the upper surface of the metal wiring layer, the protective layer having a top surface;

forming a cap layer comprising at least one material selected from the group consisting of an oxide, a nitride, a silicon–rich oxide, and an oxynitride, the cap layer disposed on the top surface of the protective layer, wherein said cap layer has [[a]] <u>no more than minor variations in</u> thickness and a composition<u>,</u> ~~which are~~ <u>the thickness and the composition</u> adapted so

that at least during a photolithographic process said cap layer creates destructive interference to reduce reflections;

forming a patterned photoresist layer on the cap layer, said patterned photoresist layer covering selected portions of the cap layer and exposing other portions of the cap layer;

etching the cap layer, the protective layer and the metal wiring layer to form the conductive structures separated by gaps; and

forming a layer of the dielectric material, comprising high density plasma chemical vapor deposition (HDPCVD) dielectric material, on surfaces exposed by the etching process including exposed surfaces of the cap layer, wherein the gaps are substantially filled with the dielectric material, and

wherein the cap layer acts to protect the wiring lines and portions of the cap layer are sacrificially removed during the process of forming the dielectric material on surfaces exposed by the etching process, wherein the protective layer comprises a material having a first dielectric constant and the cap layer comprises an antireflective coating having a second dielectric constant, different from the first dielectric constant, and wherein the first dielectric constant and the second dielectric constant form a graded index of refraction.

62. (previously presented) The method of claim 61, wherein the cap layer is used as a hard mask during etching of the wiring line layer.

63. (previously presented) The method of claim 61, wherein portions of the cap layer are partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition.

64. (previously presented) The method of claim 61, wherein the cap layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, or silicon oxynitride.

65. (previously presented) The method of claim 61, wherein the layer of dielectric material formed by HDPCVD substantially fills the gaps between the conductive structures.

66. (previously presented) The method of claim 61, wherein the layer of dielectric material formed by HDPCVD is deposited onto a surface of the substrate, onto side surfaces of the metal wiring layer, the surface layer, the protective layer, and the cap layer.

67. (previously presented) The method of claim 61, wherein the layer of dielectric material formed by HDPCVD is deposited onto an upper surface of the cap layer.

68. (previously presented) The method of claim 61, further comprising removing the patterned photoresist layer prior to forming a layer of high density plasma chemical vapor deposition (HDPCVD) dielectric material.

69. (previously presented) The method of claim 61, wherein the cap layer protects the underlying wiring layer during the process of forming a layer of high density plasma chemical vapor deposition (HDPCVD) dielectric material.

Claims 70-71. (cancelled)

72. (previously presented) The method of claim 61, wherein the graded index of refraction reduces boundary reflections between the protective layer and the antireflective coating.

73. (previously presented) The method of claim 61, wherein an antireflective coating of the cap layer reduces reflection by generating destructive interference in reflected light.

74. (previously presented) The method of claim 61, wherein twice the thickness of the cap layer is an odd number of the wavelengths of the exposure light, compensating for the dielectric constant of the cap layer.

Claims 75–77 (cancelled).

78. (previously presented) The method of claim 52, wherein the antireflective coating of the cap layer reduces reflection by generating destructive interference in reflected light.

79. (previously presented) The method of claim 50, wherein twice the thickness of the cap layer is an odd number of the wavelengths of the exposure light, compensating for the dielectric constant of the cap layer.

80. (currently amended) A method for forming conducting structures separated by gaps on a substrate comprising:

providing a substrate and a wiring line layer above the substrate;

forming a first antireflective coating above the wiring line layer;

forming a cap layer adapted for protecting the wiring line layer during a plasma based process, the cap layer being situated [[above]] on the first antireflective coating and having ~~substantially one~~ no more than minor variations in thickness, wherein the cap layer and the first antireflective coating have different dielectric constants;

forming a photoresist layer directly on top of the cap layer;

patterning the photoresist layer during a lithographic process;

etching through portions of the first antireflective coating, a portion of

the cap layer and a portion of the wiring line layer to form wiring lines separated by high aspect ratio gaps; and

depositing a dielectric material to substantially fill said gaps, including using a HDPCVD process at least until any high aspect ratio gaps are substantially filled, followed by a different plasma process that fills any remaining portion of said gaps and results in a planarized surface,

wherein the cap layer and the first antireflective coating form a graded change in an index of refraction.

81. (previously presented) The method of claim 80, wherein the first antireflective coating absorbs portions of radiation applied during the lithographic process and the cap layer creates destructive interference with portions of radiation applied during the lithographic process.

82. (previously presented) The method of claim 80, wherein the cap layer also functions as a mask during the etching process.

83. (previously presented) The method of claim 80, wherein an additional portion of the cap layer is etched while the cap layer protects the wiring line layer during the HDPCVD process.

84. (previously presented) The method of claim 80, further comprising forming a surface layer between the substrate and the wiring line layer.

85. (previously presented) The method of claim 80, further comprising the step of removing the cap layer before depositing a dielectric material within the gaps.

86. (previously presented) The method of claim 80, wherein portions of the cap layer are removed and portions of the cap layer act as a mask during the etching of the first antireflective coating and the wiring line layer.

87. (previously presented) The method of claim 80, wherein after etching each wiring line has a portion of the cap layer thereon, the portion of a cap layer on each wiring line having a cross-sectional shape selected from the group consisting of a rectangle, a triangle, trapezoid, and a rectangle having its upper corners etched away.

88. (previously presented) The method of claim 80 wherein the cap layer and the first antireflective coating are used as a hard mask.

89. (cancelled)

90. (previously presented) The method of claim 80 wherein the cap layer has a dielectric constant that is closer than a dielectric constant of the first antireflective coating to the photoresist mask layer dielectric constant.

91. (previously presented) The method of claim 80, wherein said different plasma process deposits material at a higher rate than the HDPCVD process.

92. (previously presented) The method of claim 80, wherein said different plasma process is a PECVD oxide process.

93. (previously presented) The method of claim 80, wherein the cap layer comprises silicon, oxygen, and nitrogen.

94. (previously presented) The method of claim 52, wherein a protective layer is formed on the upper surface of the metal wiring layer.

95. (previously presented) The method of claim 94, wherein the protective layer comprises a material having a first dielectric constant and the antireflective coating comprises a material having a second dielectric constant, different from the first dielectric constant.

96. (previously presented) The method of claim 95, wherein the first dielectric constant and the second dielectric constant form a graded index of refraction.

97. (previously presented) The method of claim 96, wherein the graded index of refraction reduces boundary reflections between the cap layer and the antireflective coating.

98. (previously presented) The method of claim 50, wherein the cap layer comprises silicon–rich oxide.

99. (previously presented) The method of claim 80, wherein the cap layer comprises silicon–rich oxide.

100. (previously presented) The method of claim 50, wherein a portion of the substrate is etched when the wiring lines are etched.

101. (previously presented) The method of claim 61, wherein a portion of the substrate is etched when the wiring lines are etched.

102. (previously presented) The method of claim 80, wherein a portion of the substrate is etched when the wiring lines are etched.